**Question#1: Solve the following (*4 marks*):**

**a. Suppose an 8-bit data word stored in memory is 11000010. Using the Hamming algorithm, determine what check bits would be stored in memory with the data word. Show how you got your answer?** (2.5 marks)

Data bits with value 1 are in bit positions 12, 11, 5, 4, 2, and 1:

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Poistion** | **12** | | **11** | | **10** | | **9** | | **8** | | **7** | | **6** | | **5** | | **4** | | **3** | | **2** | | **1** |
| **Bits** | **D8** | | **D7** | | **D6** | | **D5** | | **C8** | | **D4** | | **D3** | | **D2** | | **C4** | | **D1** | | **C2** | | **C1** |
| **Block** | | **1** | | **1** | | | | **0** | | **0** | | | | **0** | | **0** | | | | **1** | | **0** | | |
| **Codes** | | | | | | **1100** | | | | | | **1011** | | | | | | **0101** | | | | | | |

The check bits are in bit numbers 8, 4, 2, and 1.

Check bit 8 calculated by values in bit numbers: 12, 11, 10 and 9

Check bit 4 calculated by values in bit numbers: 12, 7, 6, and 5

Check bit 2 calculated by values in bit numbers: 11, 10, 7, 6 and 3

Check bit 1 calculated by values in bit numbers: 11, 9, 7, 5 and 3

Thus, the check bits are: 0 0 1 0

**b. For the 8-bit word 00111001, the check bits stored with it would be 0111. Suppose when the word is read from memory, the check bits are calculated to be 1101.What is the data word that was read from memory? (**2.5 marks)

The Hamming Word initially calculated was:

bit number:

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **12** | **11** | **10** | **9** | **8** | **7** | **6** | **5** | **4** | **3** | **2** | **1** |
| **0** | **0** | **1** | **1** | **0** | **1** | **0** | **0** | **1** | **1** | **1** | **1** |

Doing an exclusive-OR of 0111 and 1101 yields 1010 indicating an error in bit 10 of

the Hamming Word. Thus, the data word read from memory was 00011001.

**Question#2 (4 marks):**

**a.) Consider a memory system that uses a 28-bit address to address at the byte level, plus a cache that uses a 64-byte line size.**

**b. Assume an associative cache. If you have the address format :**

|  |  |  |
| --- | --- | --- |
|  | **S** | **W** |
| **Memory address= 28** | **22** | **6** |

**determine the following:**

**a. Number of addressable units?**

Number of addressable units = 2s+w = 228 bytes; = 268435456

**b. Number of blocks in main memory?**

number of blocks in main memory = 2s = 222= 4G blocks

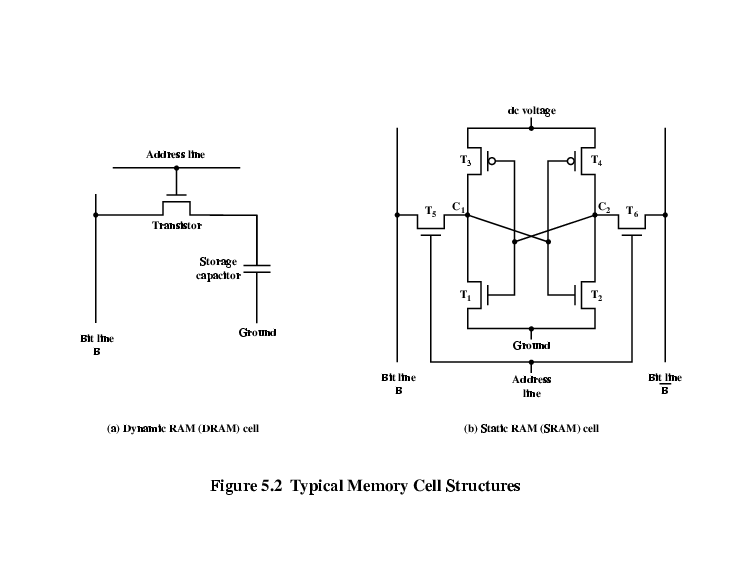
**c.Number of lines in cache?**

Number of lines in cache = undetermined

**d.Size of tag?**

Tag=28-6=22 Size of tag = 22 bits.

**Question#3 (10 marks): chose the correct answer : (1 mark each ):**

**1. At Static RAM Operation the Transistor arrangement gives stable logic state…………….: if it is:**

**C1 high, C2 low**

**T1 T4 off, T2 T3 on**

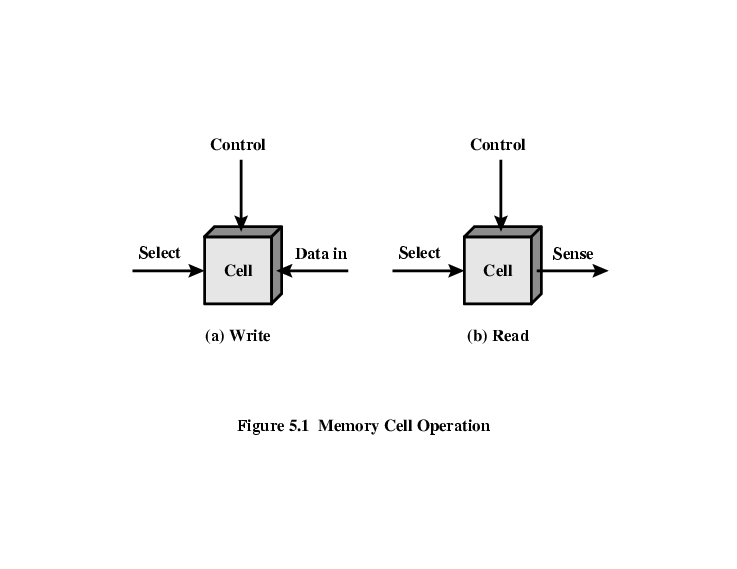
**a. State 1**

**b. State 0**

**c. toggle.**

**2. SRAM v DRAM : Both volatile**

**a. Power needed to preserve data.**

**b. Simpler to build.**

**c. does not need current.**

**3. which Memory Cell Operation ifs the flowing representation :**

**a. Read.**

**b. Write.**

**c. Rest.**

**4. We use to detected errors using Hamming error correcting code for :**

**a. Soft Error.**

**b. Hard Failure.**

**c. Permanent defect.**

**5. which DRAM can send data twice per clock cycle Rising edge of the clock pulse and falling edge.**

1. **SDRAM.**
2. **Rambus DRAM.**
3. **DDR** **SDRAM.**

**6. Cache DRAM is :**

1. **It developed by Mitsubishi**
2. **To support serial access of block of data.**
3. **All of the above .**

**7. Which mapped is has separate address spaces and need I/O or memory select lines and has an special commands for I/O and a Limited set is :**

1. **Isolated mapped I /O.**
2. **Memory mapped I/O**
3. **All of the above .**

**8. How many control/command registers to program and control DMA operation over one of its channels Intel 8237 DMA contains ?.**

1. **3 register.**
2. **4 register.**
3. **5 register.**

**9.Throw the Processor communication involves with the external device,**

**(When The I/O module accepts commands from the processor) that means :**

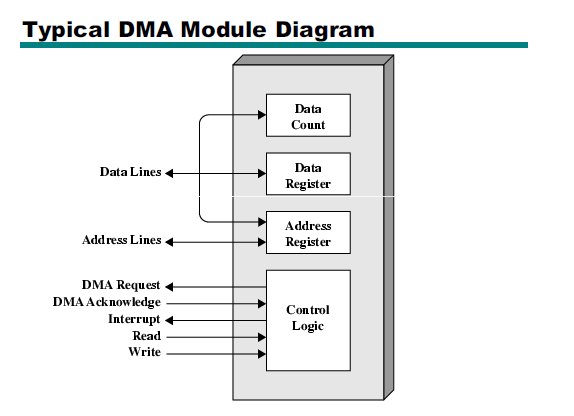
1. **Command decoding.**
2. **Status**
3. **Address recognition.**

**10. The Collection of DRAM chips Grouped into memory bank is the :**

1. **a. SDRAM.**
2. **b. Cache DRAM.**
3. **c. Interleaved Memory.**

**Question#4 (2 marks):complete the diagram with the suitable names**

**Complete the flowing diagram for DMA module diagram :**

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Good luck

Ms.Bahiya